Fig. 3 shows a partial cross-sectional view of a portion of a second embodiment of the gettering plug 108, taken along line 2-2 in Fig. 1. Like Fig. 2, Fig. 3 shows a portion of the SOI wafer 100, including the silicon active layer 102, the buried oxide layer 110 and the silicon substrate 112. Fig. 3 indicates by vertical dashed lines the approximate area of the scribe lane 106, and includes the gettering plug 108. The gettering plug 108 is separated from the silicon active layer 102, and thereby from the die pads 104 and the semiconductor devices thereon, by a sidewall liner 114. In Fig. 3, the gettering plug 108 extends through the silicon active layer 102, down to but not through the dielectric insulation layer 110 of the SOI wafer 100.

A2 cont.

A version of the above amended paragraphs marked to indicate the specific amendments may be found in the attached Appendix, in accordance with 37 CFR 1.121(b)(1).

In the Claims:

Please amend claims 2, 3 and 10-14 to read as follows:

2. (Amended) The method of claim 1, wherein the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and a dopant in the cavity.

A3

3. (Amended) The method of claim 2, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

10. (Amended) The method of claim 9, wherein the dopant is one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

A4

12. (Amended) The method of claim 9, wherein the fill material is polysilicon, and the dopant is added by one of codeposition and implantation.

A4

13. (Amended) The method of claim 9, wherein the gettering plug extends through the silicon active layer, and contacts a dielectric insulation layer on the wafer.

14. (Amended) The method of claim 9, wherein the gettering plug extends through both the silicon active layer and a dielectric insulation layer on the wafer.

Please add the following new claims 21-25:

A5

21. (New) A method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer, buried oxide layer and a silicon substrate, the silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming a plurality of cavities through the silicon active layer and the buried oxide layer to the silicon substrate in the at least one scribe lane;

filling the cavities with a fill material;

implanting at least one dopant into the fill material in the cavities to form at least one gettering plug including a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

22. (New) The method of claim 21, wherein in the gettering step, gettered impurities move into the silicon substrate.